# SSC8033GS6B

## P-Channel Enhancement Mode MOSFET

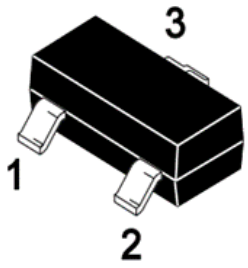
### ➢ Features

| $V_{DS}$ | $V_{GS}$ | $R_{DS(ON)}$ Typ. | $I_D$ |
|---|---|---|---|
| -30V | ±20V | 57mΩ@-10V | -4A |
| | | 80mΩ@-4V5 | |

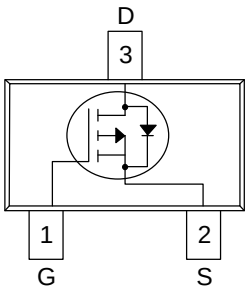
### ➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

### ➢ Pin configuration



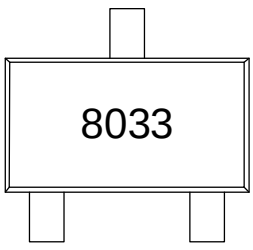

**SOT-23**




**Pin Configuration (Top View)**

### ➢ Applications

- TFT panel power switch
- Portable DVD, DPF
- High side DCDC converter
- High side driver for brushless DC motor




**Marking**

### ➢ Ordering Information

| Device | Package | Shipping |
|---|---|---|
| SSC8033GS6B | SOT-23 | 3000/Reel |

## ➢ Absolute Maximum Ratings ($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | -30 | V |
| $V_{GSS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current [a] | -4 | A |
| $I_{DM}$ | Pulsed Drain Current [b] | -16 | A |
| $P_D$ | Power Dissipation [c] | 1.44 | W |
| $T_J$ | Operation junction temperature | -55~150 | ℃ |
| $T_{STG}$ | Storage temperature range | -55~150 | ℃ |

## ➢ Thermal Resistance Ratings ($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance [a] | 87 | ℃/W |

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz.copper, in a still air environment with $T_A$=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

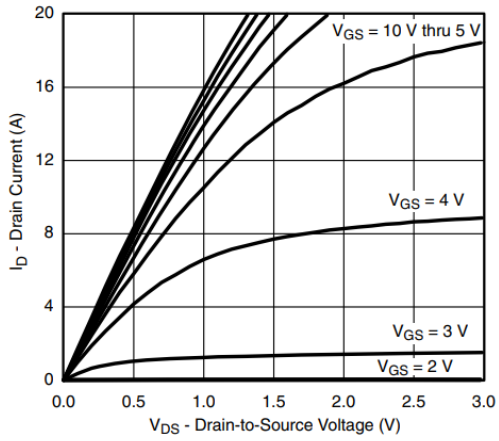
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

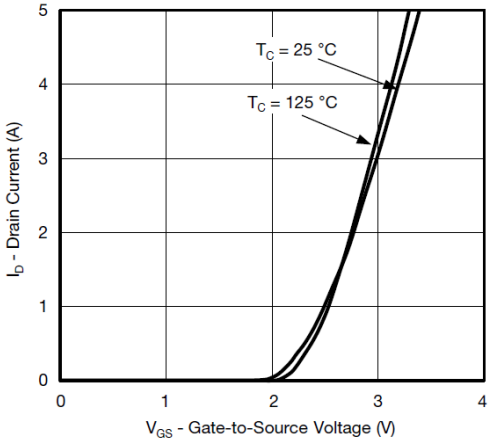
## ➢ Electrical Characteristics ($T_A$=25℃ unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250μA | -30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250uA | -1 | -1.6 | -2 | V |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$ = -10V, $I_D$ = -3A | | 57 | 80 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -2A | | 80 | 110 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -30V, $V_{GS}$ = 0V | | | -1 | μA |
| Gate-Source Leak Current | $I_{GSS}$ | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| Transconductance | $G_{FS}$ | $V_{DS}$ = -5V, $I_D$ = -2.8A | | 6 | | s |
| Forward Voltage | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = -1A | -0.6 | -0.8 | -1.3 | V |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = -15V, $V_{GS}$ = 0V, f = 1MHz | | 680 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 72 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | 58 | | |
| Turn-on Delay Time | $T_{D(ON)}$ | $V_{GEN}$ = -10V, $V_{DS}$ = -15V, $R_L$ = 6Ω, $R_G$ = 3Ω | | 10 | | ns |
| Rise Time | $T_r$ | | | 9 | | |
| Turn-off Delay Time | $T_{D(OFF)}$ | | | 33 | | |
| Fall Time | $T_f$ | | | 22 | | |
| Total Gate Charge | $Q_G$ | $V_{GS}$ = -10V, $V_{DS}$ = -15V, $I_D$ = -4A | | 12 | | nC |
| Gate to Source Charge | $Q_{GS}$ | | | 2 | | |
| Gate to Drain Charge | $Q_{GD}$ | | | 3 | | |

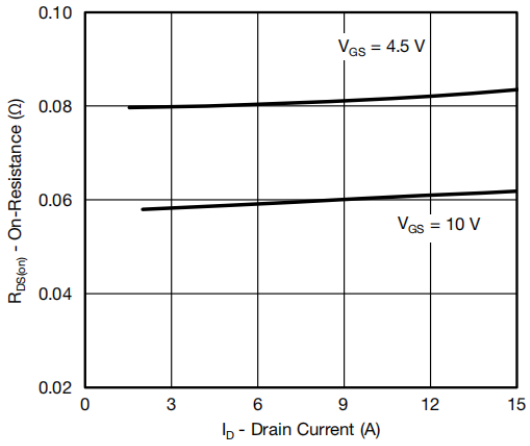
## ➢ Typical Performance Characteristics ($T_A$=25℃ unless otherwise noted)



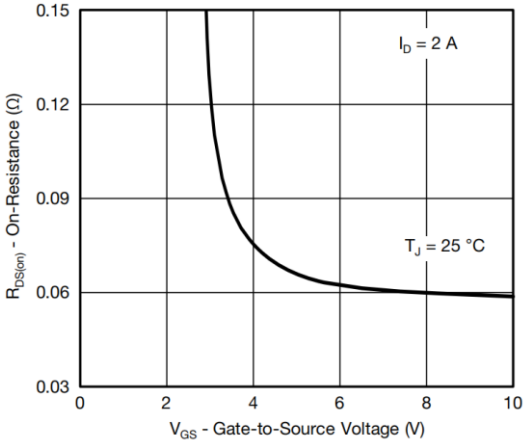

**Output Characteristics**



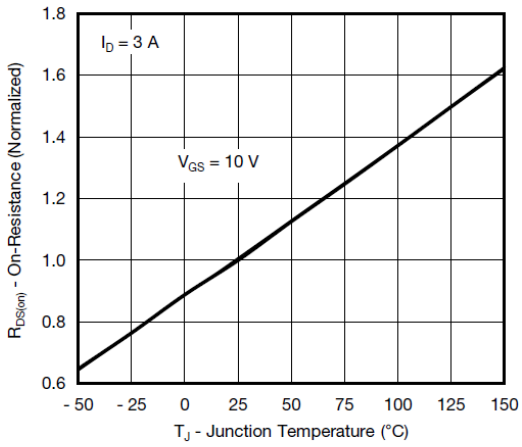

**Transfer Characteristics**



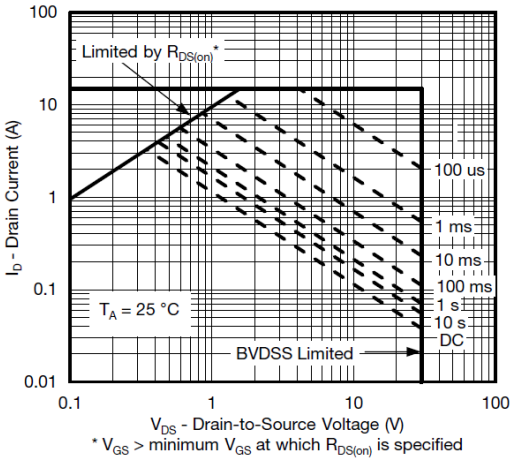

**On-Resistance vs. Drain Current**



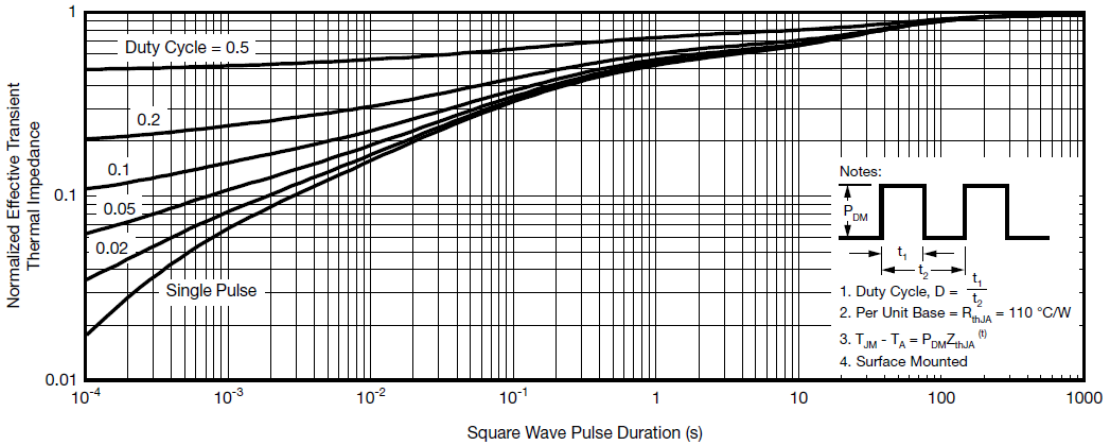

**On-Resistance vs. Gate-to-Source Voltage**




**On-Resistance vs. Junction Temperature**

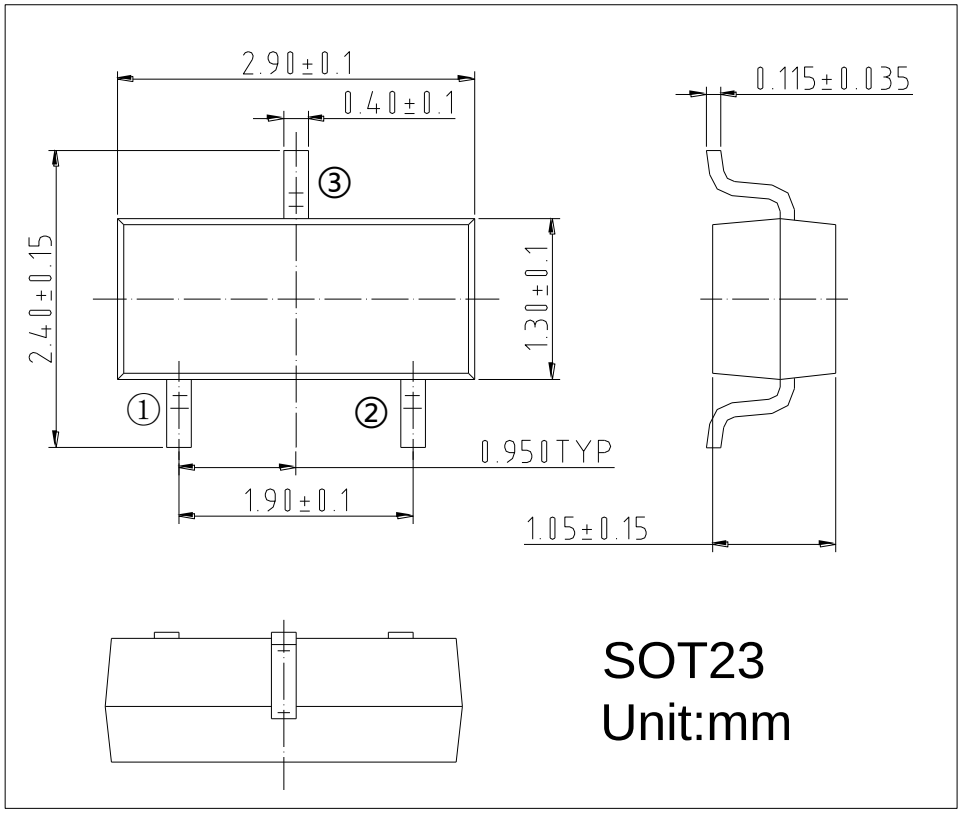



**Safe Operating Area, Junction-to-Ambient**

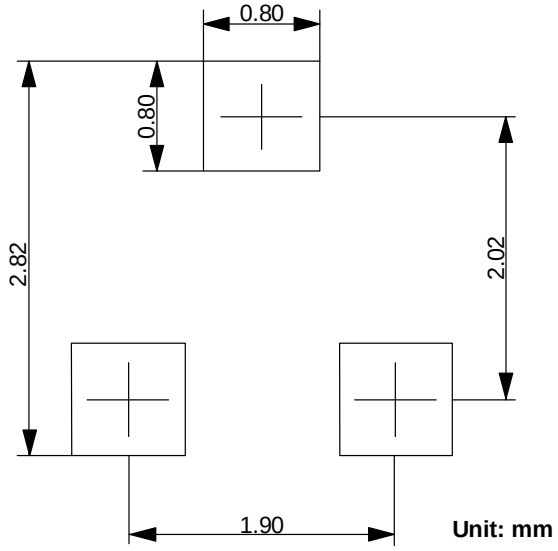



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

## ➢ Package Information




## ➢ Suggested Pad Layout



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